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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/932,086 | 08/17/2001 | Georg Farkas | CH 000018 | 5457 |

24737 7590 03/23/2006

PHILIPS INTELLECTUAL PROPERTY & STANDARDS
P.O. BOX 3001
BRIARCLIFF MANOR, NY 10510

| EXAMINER | |
|---|---|
| LAMARRE, GUY J | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2133 | |

DATE MAILED: 03/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/932,086 | FARKAS ET AL. | |
| | Examiner | Art Unit | |
| | Guy J. Lamarre | 2133 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *18 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *2,4 and 10-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,4 and 10-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### Response to Amendment

1. This office action is in response to Applicants' amendment of *18 Nov. 2005*.

1.1 **Claim 14 is** added, **Claims 2, 4** and **10-14** remain pending.

1.2 The prior art rejections of record are withdrawn in response to Applicants' amendment.

### Response to Arguments

2. Applicants' arguments are moot in view of new ground of rejection via **Abramovici et al.** ***"Digital Systems Testing and Testable Design,'*** 1990, Pgs. 479-487 and **NN74091034:** ***"Circuit Diagnosis and Design Analysis System;"*** IBM Tech. Discl. Bulletin, July 1987, US, VOL. 17 ISSUE: 4 Pgs: 1034 - 1035 ; September 1, 1974 (hereinafter **IBM Tech**).

### Claim Rejections - 35 USC ' 103

3. **Claims 2, 4** and **10-14** are rejected under 35 U.S.C. 103(a) as being unpatentable over as being unpatentable over **Abramovici et al.** and **IBM Tech.**

**As per Claims 2, 4** and **10-14, IBM Tech** substantially discloses an *external tester 60* that generates logic test patterns/vectors to test/diagnose the logic circuitry of plural semiconductor *chips 120* to enable fault localization. **Not specifically described** in detail in **IBM Tech** is the approach whereby external external tester is of programmable test generation type. **However Abramovici et al.,** in an analogous art, discloses *"Digital Systems Testing and Testable Design,"* wherein such techniques are described. {See **Abramovici et al.,** Id., Pgs. 479-487, wherein, e.g., shift registers are programmed (or PRPG: at page 483) via seed values to generate test patterns/sequences for test application thereof to the device under test.} **Therefore,** it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure in **IBM Tech** by including therein programmable test pattern circuitry for external application of test data as taught by **Abramovici et al,** because such

modification would provide the procedure disclosed in **IBM Tech** with a technique whereby "*TPG (test pattern generation) is external to the semiconductor and hence not part of the functional circuitry. ...*" to also thereby reduce tester hardware overhead. {See **Abramovici et al,** page 481 : last sentence.}

**Abramovici et al.** discloses equivalent test sequencing/output response analysis/ compression (e.g., via MISR: at page 483) , e.g., on pages 477, 481, and 483.

## Conclusion

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks, Washington, D.C. 20231

**or faxed to:** (703) 872-9306 for all formal communications.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Guy J. Lamarre, P.E., whose telephone number is (571) 272-3826. The examiner can normally be reached on Monday to Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert De Cady, can be reached at (571) 272-3819.

Information regarding the status of an application may also be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Guy J. Lamarre, P.E
Primary Examiner
3/6/2006